line 15, replace "designed" with --in a design--.

page 10, line 9, "related to the" with --in an--.

line 16, between "has" and "determined", insert --been--.

line 16, between "the" and "gate", insert --layout of the--.

line 20, replace "till" with --before--.

line 21, delete "to take".

line 24, replace "a" with --the--.

page 11, line 3, between "the" and "IC", insert --designer of the --.

line 5, delete "being".

line 5, after "maintained", insert --.--.

line 6, replace "and designing and fabricating" with --That is,--.

line 7, between "block 34" and "changed" insert --is--.

line 8, replace "terminated" with --completed--.

line 21, between "the" and "embodiment", insert --disclosed--.

line 24, replace "this." with --this embodiment.--.

line 25, delete "even".

page 12, line 2, between "chip" and "small", insert --having a--.

line 2, delete "in".

In the Claims:

Subt B'

Please amend the claims as follows:

1. (Amended) A method of manufacturing a semiconductor integrated circuit comprised of a plurality of functional blocks and a gate array block, each of the plurality of functional blocks being respectively provided with predetermined functions

a 3

by [arbitrarily-placed] semiconductor devices, the method comprising the [following] steps of:

[a first step for] placing the gate array [a basic cell] block comprised of a plurality of basic cells arranged in line and the [a] plurality of functional blocks within a predetermined area of a semiconductor chip;

[a second step for] designing [necessary] circuits for inclusion in the gate array [basic cell] block; and

[a third step for electrically connecting] establishing electrical connections between the basic cells [lying] within the gate array [basic cell] block by using interconnections according to the circuits designed in the previous step.

2. (Amended) A method of manufacturing a semiconductor integrated circuit according to [with] claim 1, wherein said gate array [basic cell] block is laid out by a standard cell system.

3. (Amended) A method of manufacturing a semiconductor integrated circuit according to [with] claim 1, wherein said first step is laid out by one of a standard cell system and [or] a full custom system.

4. (Amended) A method of manufacturing a semiconductor integrated circuit according to [with] claim 2, wherein said first step is laid out by one of a standard cell system and [or] a full custom system.

5. (Amended) A method of manufacturing a semiconductor integrated circuit according to [with] claim 1[, said third step is included electrically connecting] comprising the further steps of establishing electrical connections between the [said]

functional blocks and establishing electrical connections between the functional block and the gate array block by using interconnections.

6. (Amended) A semiconductor integrated circuit comprising:

a plurality of functional blocks placed on a semiconductor chip, said functional blocks being respectively provided with predetermined functions by [arbitrarily-placed] semiconductor devices; and

a gate array [basic cell] block placed on said chip, said gate array block being comprised of a plurality of basic cells arranged in line and electrically connected between the basic cells lying within the gate array [basic cell] block by [using] interconnections [according to a desired function for implement the] implementing a desired function, the gate array block having a circuit designed after placing said plurality of functional blocks and said plurality of basic cells on said chip.

7. (Amended) A semiconductor integrated circuit according to [with] claim 6, wherein said functional blocks and said gate array [basic cell] block are [is] laid out in a first area including a center position in a surface of said semiconductor chip [device].

8. (Amended) A semiconductor integrated circuit according to [with] claim 7, wherein said first area is surrounded with a second area comprising [made up of] a plurality of I/O buffers.

9. (Amended) A semiconductor integrated circuit according to [with] claim 6, wherein a connection [connecting] between basic cells is in accordance with a [used by] standard cell system.

Please add the following new claims: